

## 1. Features

- RF Ceramic Bandpass Filter
- Usable bandwidth 110 MHz at Fc 2850 MHz
- RoHS Compliant

**RoHS/RoHS2**  
**(2015/863/EU) Compliant**

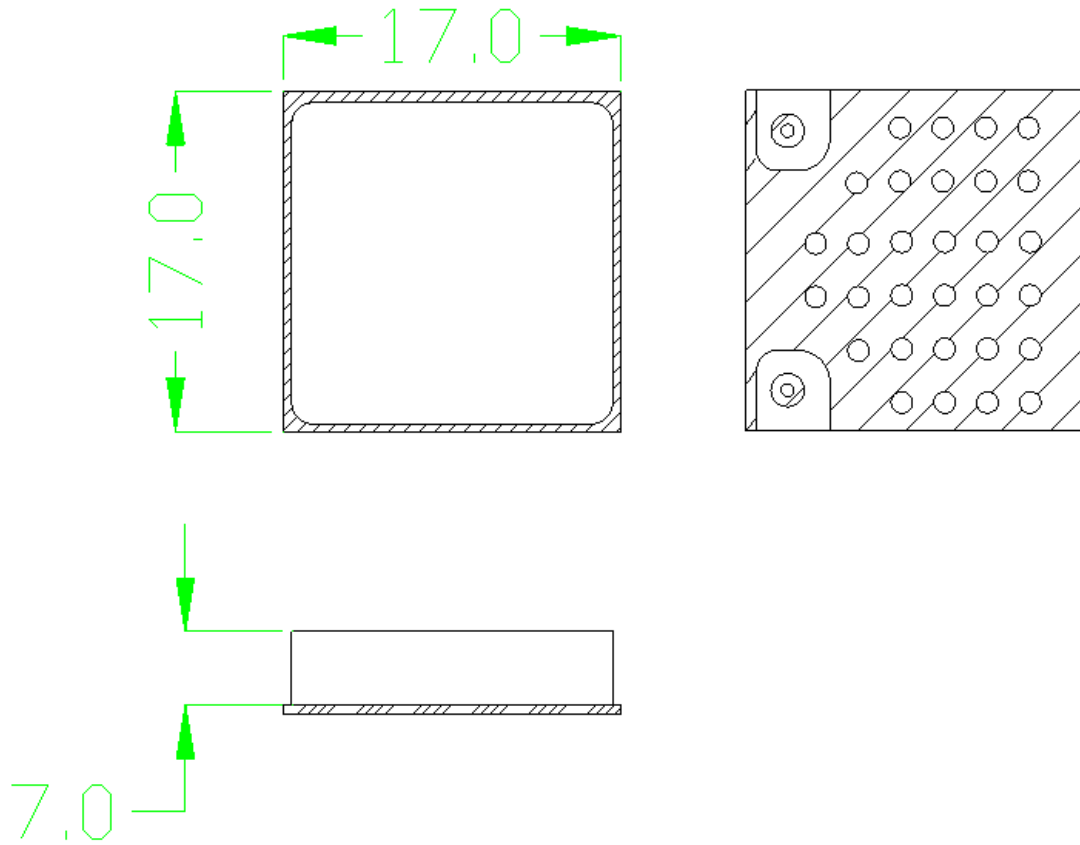
## 2. Preliminary Electrical Specifications

		Minimum	Typical	Maximum
Center Frequency (Fc)	MHz		2850	
Insertion Loss <sup>1)</sup>	dB	-	1.7	2.0
Ripple (2795 - 2905 MHz)	dB	-	0.4	0.5
Return Loss (2795 - 2905 MHz)	dB	15	16	-
Attenuation (DC - 1100 MHz)	dBc	70	75	-
Attenuation (1101 - 2100 MHz)	dBc	60	65	-
Attenuation (2101 - 2300 MHz)	dBc	45	50	-
Attenuation (2301 - 2580 MHz)	dBc	30	35	-
Attenuation (2581 - 2630 MHz)	dBc	20	25	-
Attenuation (3050 - 3200 MHz)	dBc	15	20	-
Attenuation (3201 - 3500 MHz)	dBc	30	35	-
Attenuation (3501 - 6000 MHz)	dBc	50	53	-
Input/Output Impedance	Ohm	-	50	-
Operating Temperature Range	°C	-40		+85
Power handling(CW)	dBm			30
Power handling(Instantaneous Peak)	dBm			33 (1% duty cycle, 1us pulsewidth)

1) Insertion Loss at Center frequency

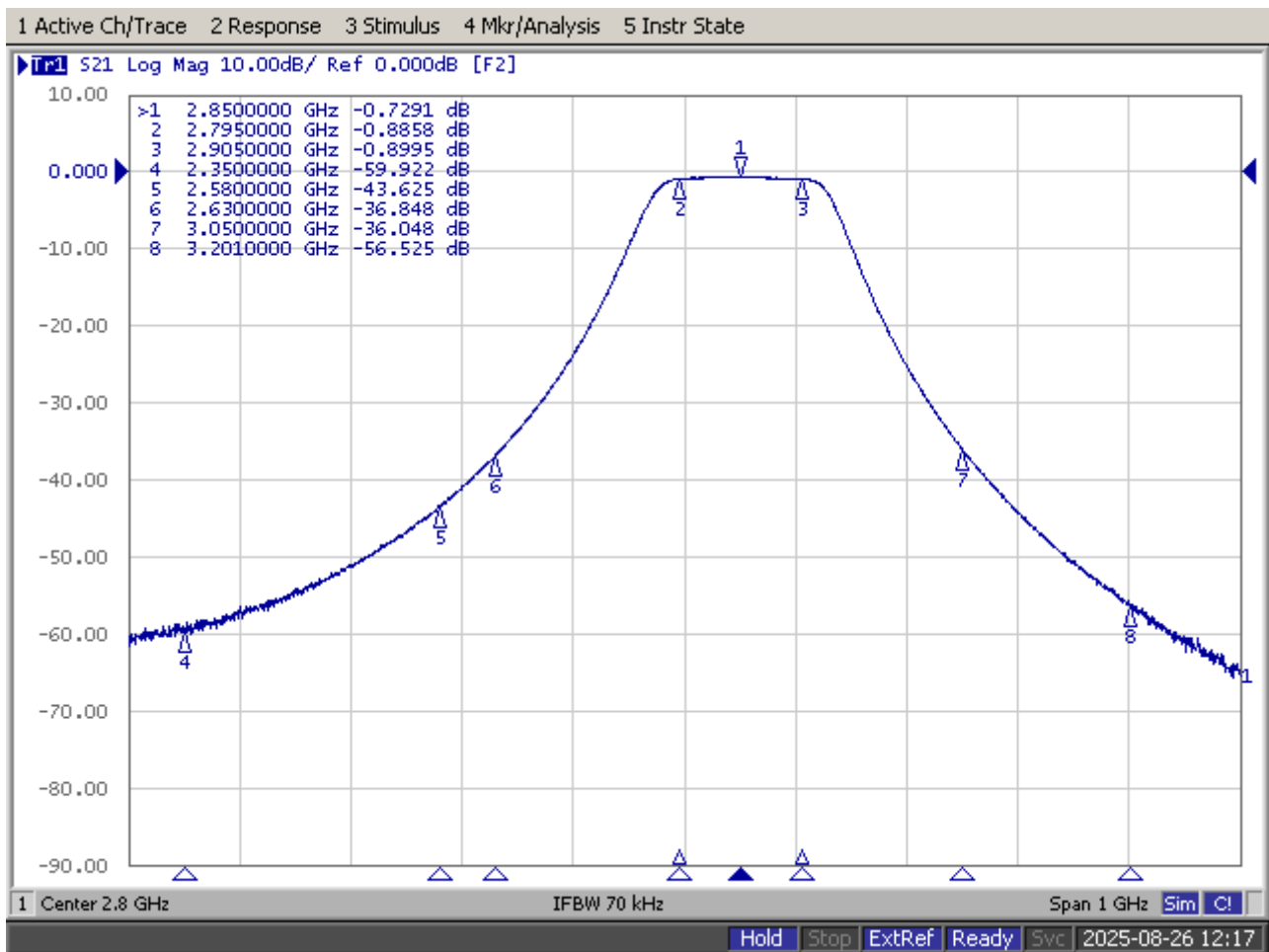
- \* All specifications are based on simulation data and ITF reserves the right to amend the specification once sample filters are produced.
- \* Actual electrical characteristics may vary due to user's PCB layout and parasitic.
- \* Ref. Meas Data.

3. Dimension (17.0 × 17.0 × 7.0 mm)

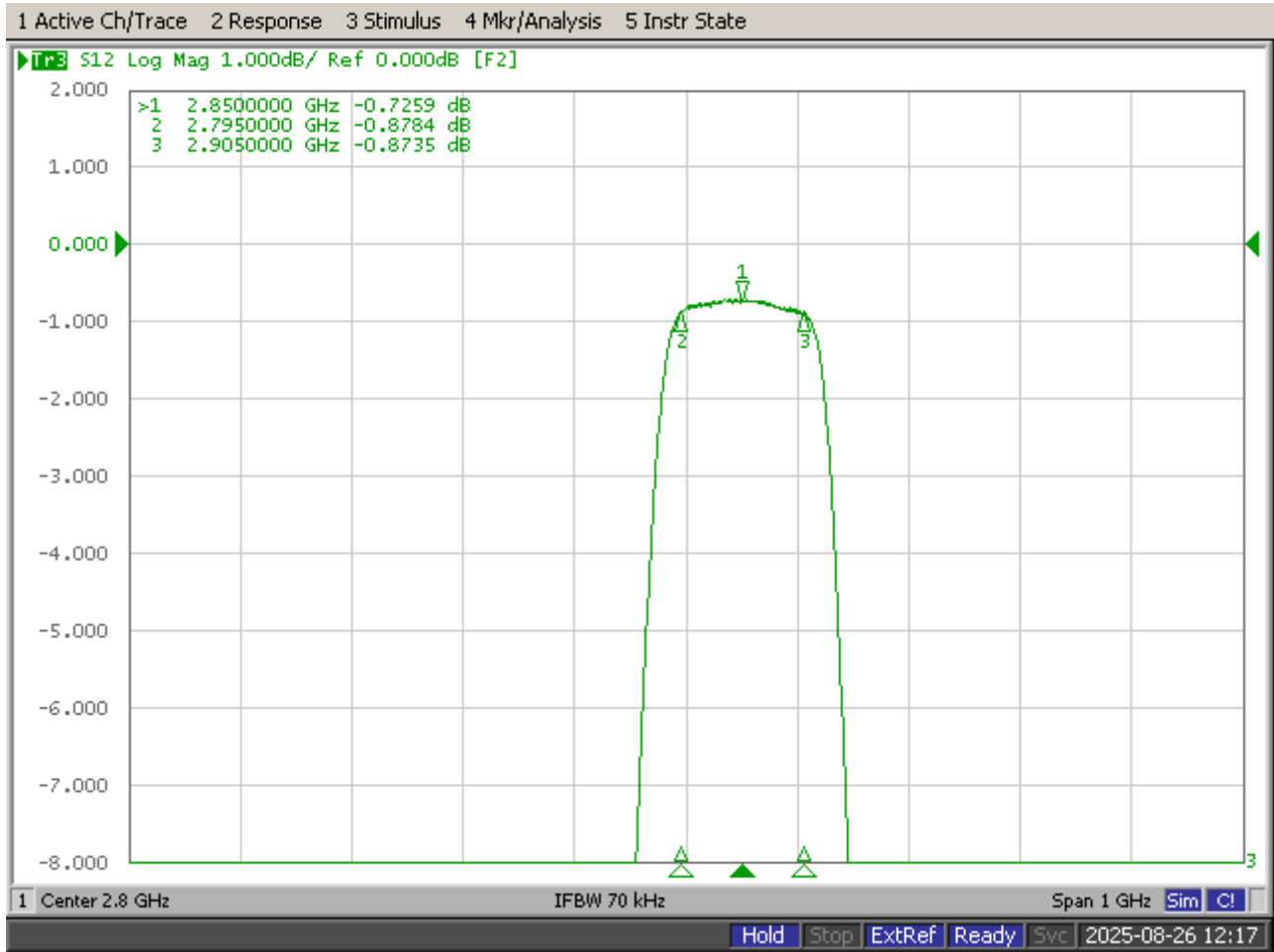


#### 4. Frequency Response (Measurement Data)

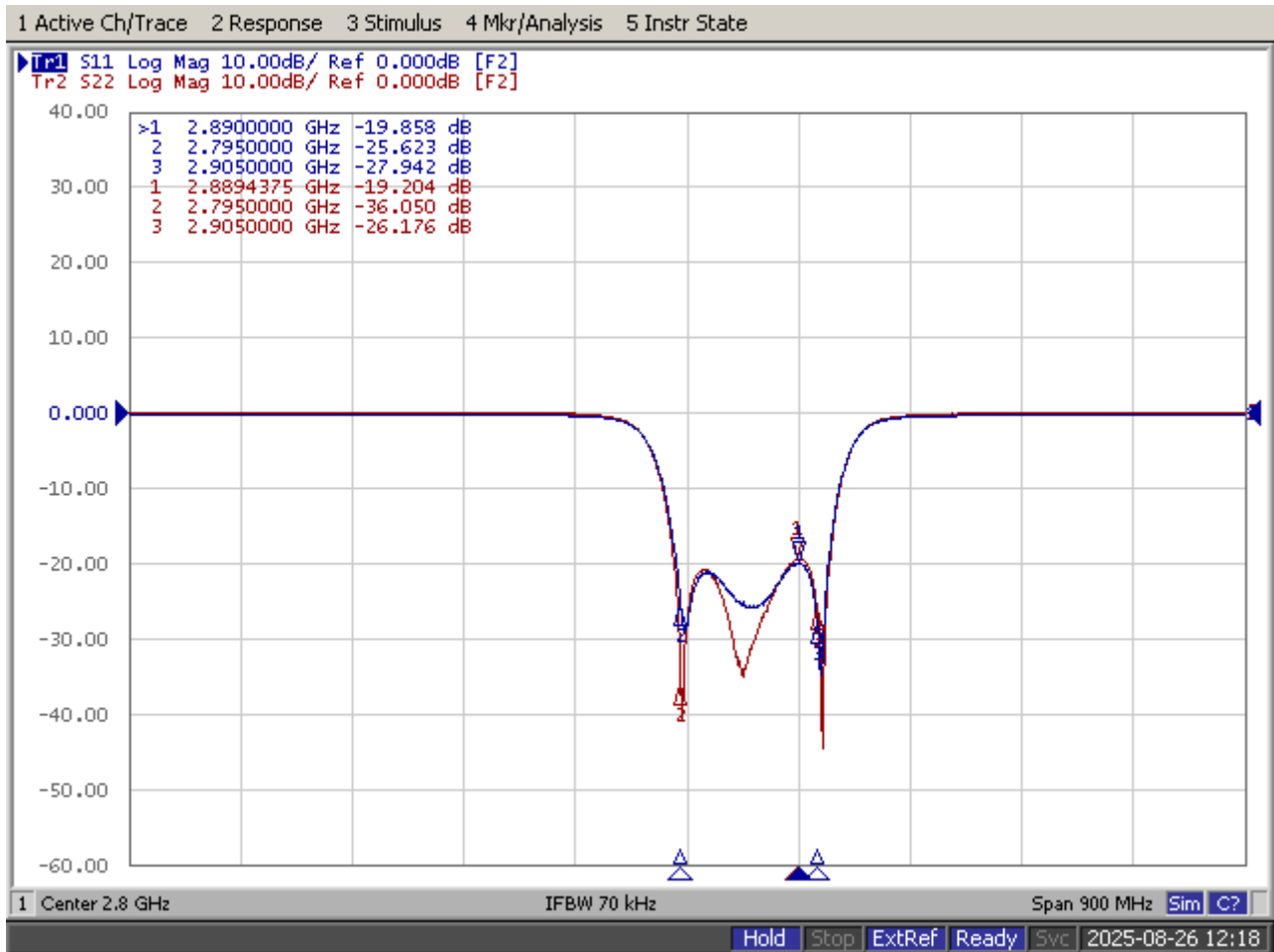
##### - Insertion loss(S21) & Attenuation



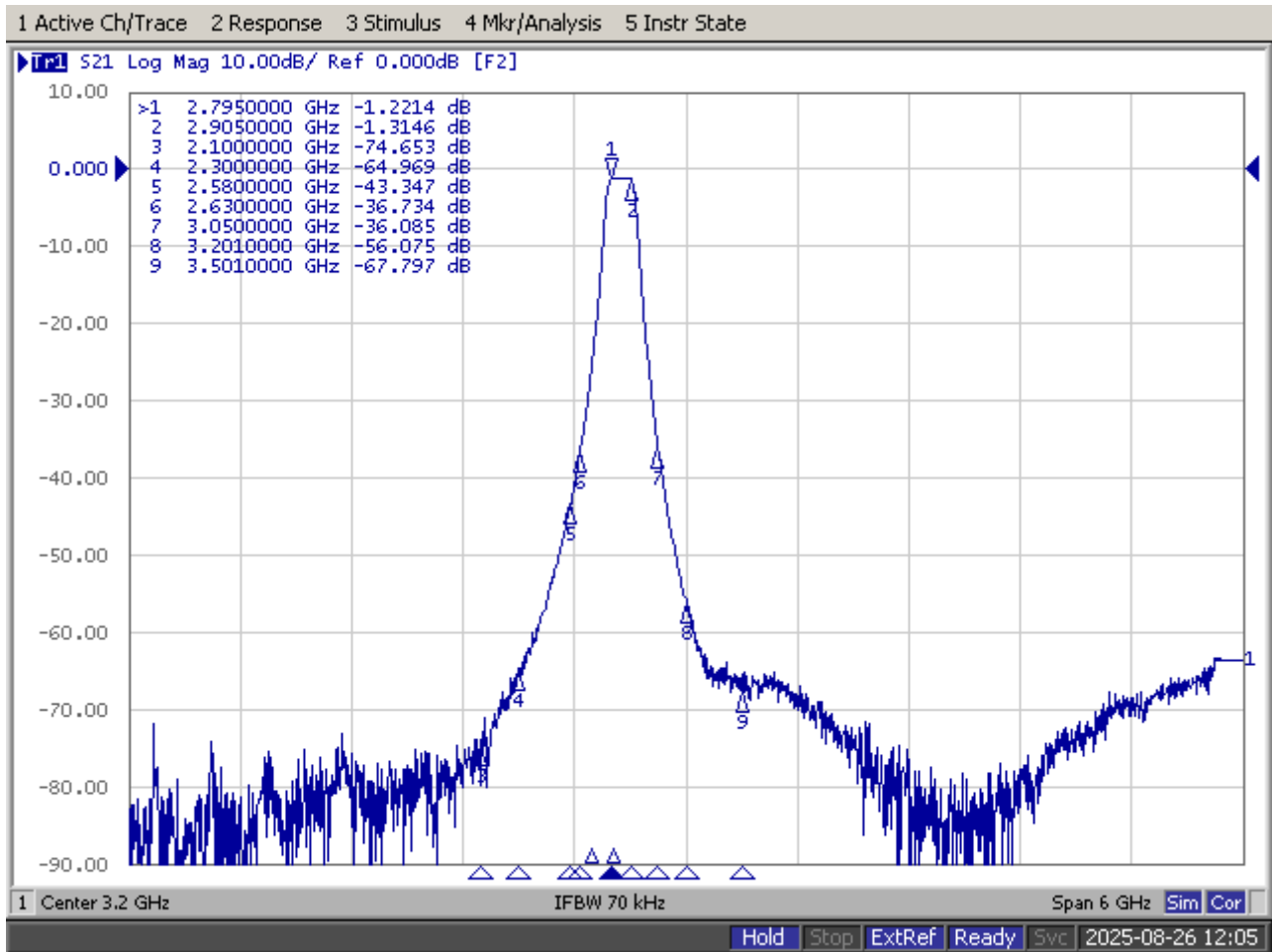
### - Ripple



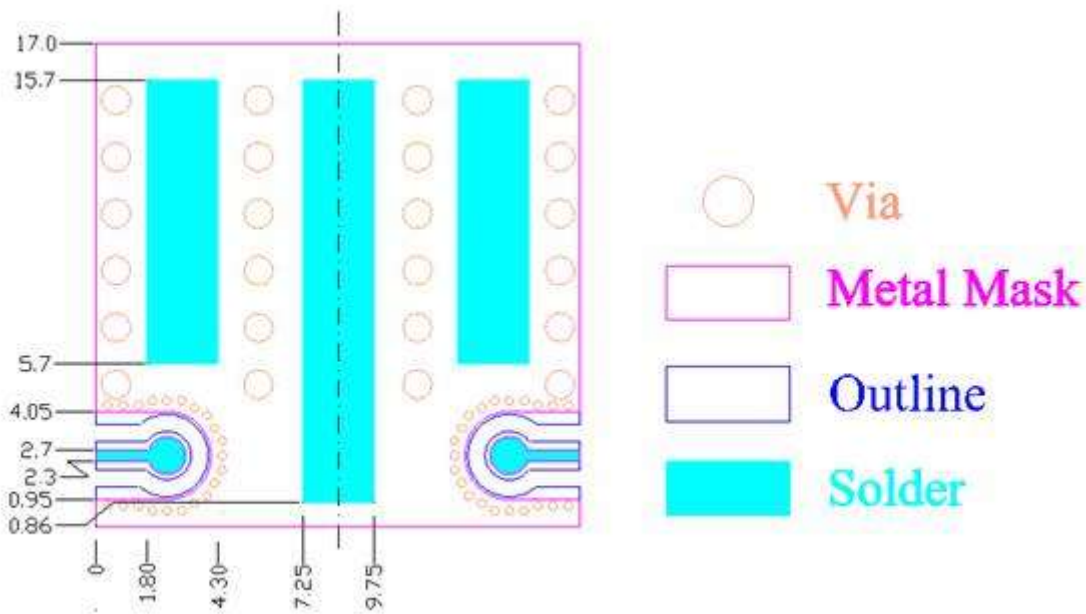
- Return Loss(S11 & S22)



- Wideband



## 5. Footprint



## A. Ground Design

- **Maintain Ground Plane Continuity:**  
Ensure continuous ground planes to minimize electrical noise and EMI.
  - **Ground Via Placement Around Critical Signal Paths:**  
Provide a sufficient number of ground vias adjacent to critical signal paths to ensure stable grounding.
  - **Recommended Via Diameter:**  
Use vias with a diameter of 0.3–0.5 mm, adjusted according to the substrate thickness.
  - **Exclusion of Ground Vias from Solder Mask Openings:**  
Do not include ground vias within solder mask openings.
  - **Ground Pattern Dimensioning:**  
Design the ground pattern to be 100-200  $\mu\text{m}$  smaller than the bottom ground pattern of the DUT to prevent alignment issues or excessive contact.
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## B. Input and Output Port Design

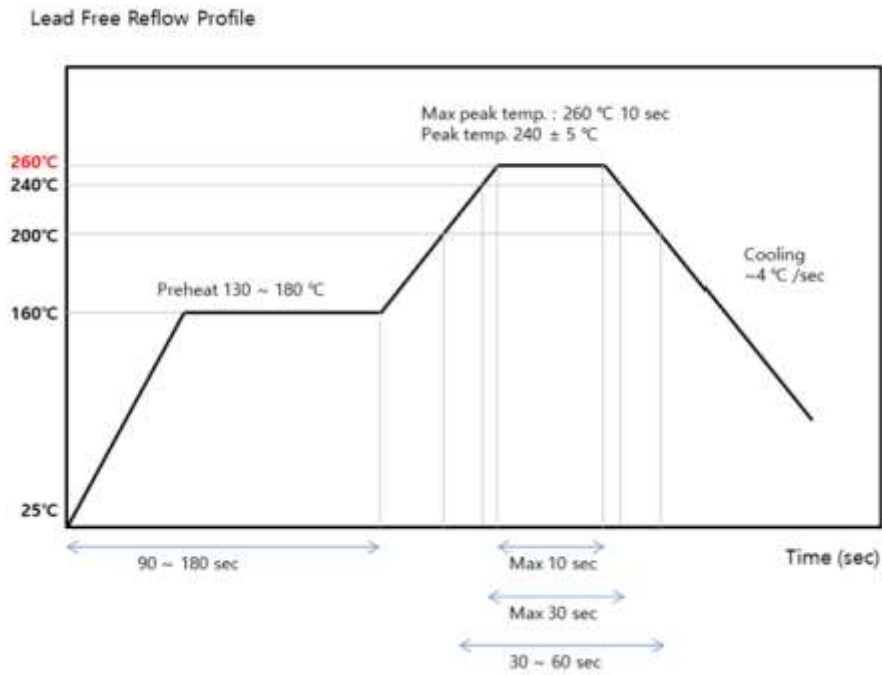
- **Optimize Signal Routing Around Ports:**  
Design signal paths near the ports for proper impedance matching and to minimize transmission losses.
  - **Via and Solder Mask Treatment:**  
Decisions on whether to remove or retain vias and solder masks near ports should be based on customer specifications.
  - **Adjustment of Trace Widths and Spacing:**  
Optimize the trace width and spacing according to the design criteria and substrate characteristics.
  - **Transmission Line and Pad Dimensioning:**  
When designing transmission lines or pads, implement them at 100-200  $\mu\text{m}$  smaller than the bottom signal pattern of the DUT to compensate for potential misalignments.
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### Note:

These guidelines should be further refined according to customer specifications and ITF's design recommendations.

## 6. Reflow profile

- Pre- Heating  $155 \pm 25^\circ\text{C}$  (90 ~120 sec.)
- Heating  $200 \pm 5^\circ\text{C}$  (30~60sec.)
- Max Peak Temperature  $260^\circ\text{C}$  (10sec. Max)



**7. Product Picture & EVB**

